HIGH FREQUENCY SEMICONDUCTOR CHIP PACKAGE AND SUBSTRATE

ABSTRACT OF THE DISCLOSURE

A substrate is configured to electrically interconnect a semiconductor chip to an external device. The substrate preferably includes a ground plane that is electrically interconnected to a ground power of the semiconductor chip. An insulating layer is attached to the ground plane. A pattern layer is attached to the insulating layer. The pattern layer includes signal patterns that communicate electrical signals with the semiconductor chip and ground patterns that are electrically interconnected to the ground plane. The ground patterns can include bonding lands to provide electrical connection to the semiconductor chip. The bonding lands can be further provided with first via holes that electrically interconnect the ground patterns to the ground plane.